PCI Express Architecture PHY Test Specification

Test Specification

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1.Introduction

This document provides test descriptions for PCI Express electrical testing. It is relevant for anyone building add-in cards or system boards to the PCI Express Card Electromechanical Specification 3.0. This specification does not describe the full set of PCI Express tests and assertions for these devices.

In particular, devices must also meet the requirements and tests described in the latest versions of the following documents as well as any other tests provided by the PCI-SIG:

PCI Express Architecture Configuration Space Test Specification

Platform BIOS Test Considerations for the PCI Express Architecture

PCI Express Architecture Link Layer Test Specification

PCI Express Architecture Transaction Layer Test Specification

1.1. Coverage

This document covers items in the PCI Express Card Electromechanical Revision 3.0 or Base Specification Revision 3.0 that apply to 8.0 GT/s, 5.0 GT/s and 2.5 GT/s signaling. 5.0 GT/s signaling requirements described in the PHY Electrical Test Consideration Revision 2.0 document apply to PCIe 2.0 devices that support 5.0GT/s and 2.5 GT/s signaling. 2.5 GT/s signaling requirements described in the PHY Electrical Test Considerations Revision 1.1 document apply to PCIe2.0, PCIe 1.1 and PCIe 1.0a devices that support 2.5 GT/s signaling.

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2. Test Descriptions

2.1. Add-in Card Transmitter Signal Quality

This test is run on all card electromechanical (CEM) form factor add-in cards. The test verifies that the signaling of the add-in card at 8.0 GT/s with selected preset transmitter equalization settings, 5.0 GT/s with 3.5 dB of de-emphasis and 5.0 GT/s with 6.0 dB of de-emphasis and 2.5 GT/s with 3.5 dB of de-emphasis meets eye diagram and other jitter requirements.

2.1.1. Starting Configuration

This test is run with devices in the polling.compliance state. This state must be supported to run the test.

2.1.2. Overview of Test Steps

The test is performed by following these steps:

1. Insert the add-in card under test into a compliance base board (CBB) revision 3.0 without power.
2. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the CBB main board are connected to receive lane zero (SMP connectors J18 and J2) on the CBB riser card via appropriate SMP to SMP cables.
3. Terminate all Tx lanes with 50 ohm terminations except the lane under test.
4. Connect the Tx lane under test to a high speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
5. Power on the CBB.
6. Push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the add-in card under test) until the compliance mode is 2.5 GT/s.
7. Perform electrical compliance test for 2.5 GT/s.

8. Push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the add-in card under test) until the compliance mode is 5.0 GT/s with 3.5 dB de-emphasis.
9. Perform electrical compliance test for 5.0 GT/s and 3.5 dB de-emphasis.
10. Push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the add-in card under test) until the compliance mode is 5.0 GT/s with 6.0 dB de-emphasis.
11. Perform electrical compliance test for 5.0 GT/s and 6.0 dB de-emphasis.
12. Perform electrical compliance test for 8.0 GT/s (see section 2.1.2).
13. Power down the CBB and remove the add-in card.

2.1.3. Add-in Card Transmitter Electrical Compliance Test for 2.5 GT/s and 5.0 GT/s

1. Measure the transmitted waveform with a high speed oscilloscope or equivalent data capture instrument.
2. Capture 1 million unit intervals of data at 5.0 GT/s and 250,000 intervals of data at 2.5 GT/s. (250,000 X 400.0ps = 100.0μs at 2.5 GT/s, 106 X 200.0ps = 200.0μs at 5.0 GT/s).
3. Measure eye amplitude and eye width using the SigTest analysis program with the appropriate (2.5 or 5.0 GT/s) add-in card template file.
4. The SigTest analysis program will also indicate if the acquired data pattern matches the expected compliance pattern. (this check is informative)
5. The test operator should confirm that the test pattern is a compliance pattern. If the pattern is a link training sequence or a clock pattern the device fails.

2.1.4. Add-in Card Transmitter Electrical Compliance Test for 8.0 GT/s

1. If the correct Transmitter Equalization setting is known push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the add-in card under test) until the correct Tx EQ is selected, otherwise, push the compliance toggle button untilthe initial 8 GT/s Tx EQ preset is selected.
2. Measure the transmitted waveform with a high speed oscilloscope or equivalent data capture instrument.
3. Capture 1.6 million unit intervals of data (1.6 X 106 X 125.0ps = 200.0μs).
4. Note: The portion of the 8.0 GT/s Add-in Card Test Channel not present on the CBB will be embedded into the captured waveform by Sigtest. The s-parameters to be embedded are included with this specification.
5. Measure eye amplitude and eye width using SigTest analysis program with the 8 GT/s add-in card test template file.(eye height 50 mV and eye width 45 ps)

Note – these limits are more constrained than the limits in the PCI Express Card Electromechanical (CEM) specification to account for the clean clock in the CBB fixture.

6. The SigTest analysis program will also indicate if the acquired data pattern matches the expected compliance pattern. (this check is informative)
7. If the SigTest analysis program indicates that the add-in card passes, the electrical compliance test is complete. If SigTest indicates the add-in card fails, the next Tx EQ setting should be selected (by pushing the compliance toggle button) and steps 2 through 6 of this test procedure should be repeated until the add-in card passes or all Tx EQ settings have been tested.

2.2. Add-in Card Transmitter Preset Test for 8.0GT/s

This test is run on all card electromechanical form factor add-in cards that operate at 8.0GT/s. The test verifies that the add-in card produces the correct transmitter equalization values for each preset in the set of 11 presets.

2.2.1. Starting Configuration

This test is run with devices in the polling.compliance state. This state must be supported to run the test.

2.2.2. Overview of Test Steps

The test is performed by following these steps:

1. Insert the add-in card under test into a CBB revision 3.0 without power.
2. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the CBB main board are connected to receive lane zero (SMP connectors J18 and J2) on the CBB riser card via appropriate SMP to SMP cables.
3. Terminate all Tx lanes with 50 ohm terminations except the lane under test.
4. Connect the Tx lane under test to a high speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
5. Power on the CBB.
6. Set add-in card to the initial 8.0 GT/s test state using the compliance toggle button on the CBB.
   Note – An alternate mechanism may be used to get to the appropriate TX compliance state.
7. Capture 1.6 million unit intervals of data (1.6 X 106 X 125.0ps = 200.0µs). Save the captured waveform to a file with a unique name to identify which preset was enabled when the waveform was captured. The captured data pattern should be compliance pattern and must contain runs of 64 ones and 64 zeros.
8. Press the compliance toggle button to cause the card under test to change to the next transmitter equalization preset value.
9. Repeat steps seven and eight until all 11 presets have been captured and saved.
10. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values must be within their specified limits.

2.3. Add-in Card Transmitter Initial TX EQ test for 8.0GT/s

This test is run on all card electromechanical form factor add-in cards that operate at 8.0GT/s. The test verifies that the add-in card will start with the correxct TX EQ preset at 8 GT/s requested through the protocol.

2.3.1. Starting Configuration

A protocol aware signal source and receiver such as a Protocol Test Card (PTC), Bit Error Ratio Tester (BERT), other specialized test equipment or any combination of different test equipment that can perform the test is connected to the device under test via a CBB. Since it is necessary to send commands to the DUT to adjust the transmitter equalization values and to get the DUT into loopback mode in order to perform this test, the test equipment must be able to perform the sequence of steps outlined in the PCI Express Base Specificantion, Rev. 3.0, sections 4.2.6.4.2 and in this document's Appendix A: Getting into Loopback for 8GT/s.

2.3.2. Overview of Test Steps

The test is performed by following these steps:

1. Insert the add-in card under test into a CBB revision 3.0 without power.
2. Connect the transmitter output of the protocol aware test equipment to the Rx SMP connectors on the CBB lane under test via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
3. Connect the 100 mhz reference clock output from the test equipment to the clock input SMP connectors on the CBB.
4. TX lanes other than the lane under test can be terminated with 50 ohm terminations or unterminated – as requested by the device under test provider.
5. Connect the Tx lane under test to signal splitters with one set of outputs going to the receiver inputs of the protocol aware test equipment and the other set of outputs going to a high speed oscilloscope or equivalent data capture instrument (if the protocol aware test equipment is capable of acquiring the signal on it's receiver and saving it to a file, the splitters and oscilloscope can be omitted). All connections to the CBB should be made via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables. All other connections should be made via phase matched, low loss SMA cables.
6. Power on the CBB.
7. Have the test equipment train the DUT and negotiate to 8.0 GT/s requesting P0 as the initial preset for the DUT. The test equipment does not request any TX EQ adjustments in phase 3.
8. Verify that the TX EQ preset for the DUT stays consistent once it transitions to 8 GT/s.
9. Have the test equipment put the DUT into loopback and transmit the compliance pattern so that it gets returned to the test equipment and oscilloscope.
10. Capture 1.6 million unit intervals of data ($1.6 \times 10^6 \times 125.0\text{ps} = 200.0\mu\text{s}$). Save the captured waveform to a file with a unique name to identify that this waveform is for preset P0..

11. Repeat the test for the equivalent of each preset from P0 to P9.
12. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values must be within their specified limits.

2.4. Add-in Card Transmitter Link Equalization Response Test for 8.0GT/s

This test is run on all card electromechanical form factor add-in cards that operate at 8.0GT/s. The test verifies that the add-in card will respond correctly to transmitter equalization commands sent via the link protocol.

2.4.1. Starting Configuration

A protocol aware signal source and receiver such as a Protocol Test Card (PTC), Bit Error Ratio Tester (BERT),other specialized test equipment or any combination of different test equipment is connected to the device under test via a CBB. Since it is necessary to send commands to the DUT to adjust the transmitter equalization values and to get the DUT into loopback mode in order to perform this test, the test equipment must be able to perform the sequence of steps outlined in the PCI Express Base Specificantion, Rev. 3.0, sections 4.2.6.4.2 and in this document's Appendix A: Getting into Loopback for 8GT/s.

2.4.2. Overview of Test Steps

The test is performed by following these steps:

1. Insert the add-in card under test into a CBB revision 3.0 without power.
2. Connect the transmitter output of the protocol aware test equipment to the Rx SMP connectors on the CBB lane under test via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
3. Connect the 100 MHz reference clock output from the test equipment to the clock input SMP connectors on the CBB.
4. TX lanes other than the lane under test can be terminated with 50 ohm terminations or unterminated – as requested by the device under test provider.
5. Connect the Tx lane under test to signal splitters with one set of outputs going to the receiver inputs of the protocol aware test equipment and the other set of outputs going to a high speed oscilloscope or equivalent data capture instrument (if the protocol aware test equipment is capable of acquiring the signal on it's receiver and saving it to a file, the splitters and oscilloscope can be omitted). All connections to the CBB should be made via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables. All other connections should be made via phase matched, low loss SMA cables.
6. Power on the CBB.
7. Have the test equipment train the DUT and negotiate to 8.0 GT/s.

8. Have the test equipment send a command to the DUT to set its transmitter equalization to preset 4.
9. Verify that the requested equalization change is complete within 1 microsecond from when the test equipment first sends the request . Note – the test equipment operator must be able to determine when the first request was sent relative to the observed TX EQ changed in the DUT. The test equipment/operator records the cursors reported by the device under test for the preset being tested.
10. Have the test equipment put the DUT into loopback and transmit the compliance pattern so that it gets returned to the test equipment and oscilloscope.
11. Capture 1.6 million unit intervals of data ($1.6 \times 10^6 \times 125.0ps = 200.0\mu s$). Save the captured waveform to a file with a unique name to identify that this waveform mimics preset four.
12. Repeat steps 6-11 for each preset from P0 to P9.
13. Use the SigTest Transmitter Preset Test option to read the ten saved waveform files and compute the preset values from these. All preset values computed must be within their specified limits.
14. The test is repeated with each request for the device under test TX equalization using the cursors reported by the device under test for that preset.
15. Repeat the test for each lane.

2.5. System Board Transmitter Signal Quality

This test is run on all card electromechanical form factor system boards. The test verifies that the signaling of the system at 2.5 GT/s, 5.0 GT/s and 8.0 GT/s with all specified transmitter equalization values meets eye diagram and other jitter requirements.

2.5.1. Starting Configuration

This test is run with devices in the polling.compliance state. This state must be supported to run the test.

2.5.2. Overview of Test Steps

The test performed by following these steps:

1. Power down the system under test.
2. Insert the compliance load board (CLB) revision 3.0 into the slot for test.
3. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the front of the CLB are connected to receive lane zero (SMP connectors JXX and JX) on the back of the CLB via appropriate SMP to SMP cables.
4. Terminate all lanes with 50 ohm terminations except the lane under test.
5. Connect the lane under test to a high speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.

6. Connect the clock signal to the high speed oscilloscope or equivalent data capture instrument via the reference clock SMP connectors on the CLB. The clock must have SSC enabled or disabled to be consistent with settings for the system during normal operation.
7. Power on the system under test.
8. Set the system to initial test state (e. g. 2.5 GT/s, -3.5dB de-emphasis).
9. Perform electrical compliance test for 2.5 GT/s and 5.0 GT/s (see section 2.5.1).
10. If the system supports the 8.0 GT/s data rate, perform electrical compliance test for 8.0 GT/s (see section2.5.2).
11. Power down the system and remove the CLB.

2.5.3. System Board Transmitter Electrical Compliance Test for 2.5 GT/s and 5.0 GT/s

1. Measure transmitted clock and data waveforms simultaneously with a high speed oscilloscope or equivalent data capture instrument.
2. Capture 1 million unit intervals of data and clock (10^6 X 400.0ps = 400.0µs at 2.5 GT/s, 10^6 X 200.0ps = 200.0µs at 5.0 GT/s).
3. Measure eye amplitude and eye width using the SigTest analysis program with the appropriate choice of template file. Template files differ based on data rate, transmitter equalization (de-emphasis) settings and the type of device under test (add-in card or system).
4. The SigTest analysis program will also indicate if the acquired data pattern matches the expected compliance pattern. (this check is informative)
5. The test operator should confirm that the test pattern is a compliance pattern. If the pattern is a link training sequence or a clock pattern the device fails.
6. Push the compliance toggle button on the CLB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the add-in card under test) until the compliance mode is either 5.0 GT/s and 3.5 dB or 5.0 GT/s and 6.0 dB – whichever will be used by the system in real operation...
7. Repeat steps 1-5.

Note – An alternate mechanism may be used to get to the appropriate TX compliance state.

2.5.4. System Board Transmitter Electrical Compliance Test for 8.0 GT/s

1. If the correct Transmitter Equalization setting is known, push the compliance toggle button on the CLB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the motherboard under test) until the correct Tx EQ is selected, otherwise push the compliance toggle button until the initial 8 GT/s Tx EQ preset is selected.
2. Measure transmitted clock and data waveforms simultaneously with a high speed oscilloscope or equivalent data capture instrument.
3. Confirm that the waveform is the correct compliance pattern.
4. Capture 1.6 million unit intervals of data (1.6 X 10^6 X 125.0ps = 200.0µs).

   Note: The portion of the 8.0 GT/s System Board Test Channel not present on the CLB will be embedded into the captured data waveform by Sigtest. The s-parameters to be embedded are included with this specification.

5. Measure eye amplitude and eye width using SigTest analysis program with the appropriate choice of template file. Template files differ based on data rate, transmitter equalization settings and the type of device under test (add-in card or system).
6. The SigTest analysis program will also indicate if the acquired data pattern matches the expected compliance pattern. (this check is informative)
7. If the SigTest analysis program indicates that the system board passes, the, electrical compliance test is complete. If SigTest indicates the system board fails, push the compliance toggle button on the CLB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the motherboard under test) to select the next Tx EQ setting and steps 2 through 7 of this test procedure should be repeated until the system board passes or all Tx EQ settings have been tested.

   Note – an alternate mechanism may be used to get to the appropriate TX compliance state.

2.6. System Board Transmitter Preset Test for 8.0GT/s

This test is run on all card electromechanical form factor system boards that operate at 8.0GT/s. The test verifies that the system board produces the correct transmitter equalization values for each preset in the set of 11 presets.

2.6.1. Starting Configuration

This test is run with devices in the polling.compliance state. This state must be supported to run the test.

2.6.2. Overview of Test Steps

The test is performed by following these steps:

1. Power down the system under test.
2. Insert the compliance load board revision 3.0 into the slot to be tested.
3. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the front of the CLB are connected to receive lane zero (SMP connectors JXX and JX) on the back of the CLB via appropriate SMP to SMP cables.
4. Connect the Tx lane under test to a high speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
5. Power on the system under test.
6. Set system to the initial 8.0 GT/s test state using the compliance toggle button on the CLB.

7. Capture 1.6 million unit intervals of data (1.6 X 106 X 125.0ps = 200.0µs). Save the captured waveform to a file with a unique name to identify which preset was enabled when the waveform was captured. The captured data pattern should be compliance pattern and must contain runs of 64 ones and 64 zeros.Press the compliance toggle button to cause the system under test to change to the next transmitter equalization preset value.
8. Repeat steps seven and eight until all 11 presets have been captured and saved.
9. Power down the system and remove the CLB.
10. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values must be within their specified limits.

2.7. System Board Transmitter Link Equalization Response Test for 8.0GT/s

This test is run on all card electromechanical form factor system boards that operate at 8.0GT/s. The test verifies that the system will respond correctly to transmitter equalization commands sent via the link protocol.

2.7.1. Starting Configuration

A protocol aware signal source and receiver such as a Protocol Test Card (PTC), Bit Error Rate Tester (BERT) or other specialized test equipment is connected to the device under test via a CLB. Since it is necessary to send commands to the DUT to adjust the transmitter equalization values and to get the DUT into loopback mode in order to perform this test, the protocol aware test equipment must be able to perform the sequence of steps outlined in the PCI Express Base Specificantion, Rev. 3.0, sections 4.2.6.4.2 and in this document's Appendix A: Getting into Loopback for 8GT/s.

2.7.2. Overview of Test Steps

The test is performed by following these steps:

1. Power down the system under test.
2. Insert the CLB revision 3.0 into the system under test.
3. Connect the transmitter output of the protocol aware test equipment to the Rx SMP connectors on the CLB lane under test via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables..
4. TX lanes other than the lane under test can be terminated with 50 ohm terminations or unterminated – as requested by the device under test provider.
5. Connect the Tx lane under test to signal splitters with one set of outputs going to the receiver inputs of the protocol aware test equipment and the other set of outputs going to a high speed oscilloscope or equivalent data capture instrument (if the protocol aware test equipment is capable of acquiring the signal on it's receiver and saving it to a file, the splitters and oscilloscope can be omitted). All connections to the CLB should be made via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables. All other connections should be made via phase matched, low loss SMA cables.

6. Power on the system under test.
7. Have the test equipment train the DUT and negotiate to 8.0 GT/s.
8. Have the test equipment send a command to the DUT to set the transmitter to preset 4 (preshoot to 0.0dB and de-emphasis to 0.0dB).
9. Verify that the requested equalization change is complete within 1 microsecond from when the test equipment first sends the request . Note – the test equipment operator must be able to determine when the first request was sent relative to the observed TX EQ changed in the DUT.
10. Have the test equipment put the DUT into loopback and transmit the compliance pattern so that it gets returned to the test equipment and oscilloscope.
11. Capture 1.6 million unit intervals of data (1.6 X 106 X 125.0ps = 200.0μs). Save the captured waveform to a file with a unique name to identify that this waveform mimics preset four.
12. Repeat steps 6-11 with each additional preset from P0 to P9.
13. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values computed must be within their specified limits.
14. The test is repeated with each request for the device under test TX equalization using the cursors reported by the system under test for that preset.
15. Repeat the test for each lane.

2.8. Add-in Card Receiver Jitter Tolerance Test

This test is run on all card electromechanical form factor add-in cards. The test verifies that the add-in card can function normally in systems with jitter near the specification allowed limits and does not exceed the allowed receiver error rate in loopback mode.

Note: The test equipment error detector shall ignore SKP ordered sets when counting errors.

2.8.1. Starting Configuration

A programmable signal source such as a Bit Error Rate Tester (BERT), Arbitrary Waveform Generator (AWG) or other specialized test equipment is connected to the device under test (DUT) via a compliance base board. Since it is necessary to get the add-in card into loopback mode in order to perform this test, the signal source must be able to perform the sequence of steps outlined in Appendix A: Getting into Loopback for all data rates supported by the device under test.

Calibration is done by connecting a CLB to a CBB. For add-in cards, the CLB takes the place of the DUT for calibration purposes thus the signal is monitored at the Tx SMP connectors for lane 0 of the CLB.

2.8.2. Overview of Calibration Steps

The calibration is performed by following these steps:

1. Connect the end of the cables that will connect to the RX SMPs on the add-in card test fixture as directly as possible (if any adaptors are used they must be minimal loss) to a real time oscilloscope and the other end to the test equipment generator and differential mode noise solution.
2. Have the test equipment transmit a pattern with 64 ones followed by 64 zeros followed by 128 bits of a 1010 clock pattern at 8 GT/s.
3. Measure the transmitted signal on the oscilloscope and adjust the post cursor de-emphasis and swing of the generator until the low frequency and high frequency portions of the signal have an equal differential amplitude of 800 mV peak to peak..
4. Adjust the Rj source of the test equipment to target approximately 1.5 ps RMS. The Rj is applied over the frequency range defined in the PCI Express 3.0 Base Specification section 4.3.4.4.1.
5. Capture 1.6 million unit intervals of data with a 1010 clock pattern (1.6 X 106 X 125.0ps = 200.0μs). Save the captured waveform to a file.
6. Analyze the waveform just captured using SigTest and the template for Gen 3 system RX calibration. Note the amount of spectrally flat Rj.
7. If the computed Rj is not within the calibration limits of 1.5 +.2/-0 ps RMS, readjust the Rj value on the generator accordingly and repeat steps 8 through 9. Note that Rj will be adjusted again in final adjustments to achieve the target eye height and width.
8. Note the Rj setting on the generator so that it can be recalled later.
9. Turn all jitter and noise sources off.
10. Have the test equipment transmit the Gen 3 compliance pattern with no noise or jitter sources turned on.
11. Capture 1.6 million unit intervals of data (1.6 X 106 X 125.0ps = 200.0μs). Save the captured waveform to a file.
12. Analyze the waveform just captured using SigTest and the template for RX calibration (does not apply the reference equalizer). Note the amount of Tj (total jitter) found by SigTest.
13. Adjust the 100 Mhz Sj (sinusoidal jitter) component of the generator to approximately 0.1UI (12.5 ps).
14. Capture 1.6 million unit intervals of data (1.6 X 106 X 125.0ps = 200.0μs). Save the captured waveform to a file.
15. Analyze the waveform just captured using SigTest and the template for Gen 3 RX calibration. Note the amount of Tj. The amount of Sj is found by subtracting the Tj found in step 6 above from the Tj just computed.
16. If the computed Sj is not within calibration limits of 12.5 +1/-0 ps , readjust the Sj value on the generator accordingly and repeat steps 14 through 15.
17. Note the Sj setting on the generator so that it can be recalled later.
18. Turn all jitter sources off.

19. Connect a revision 3.0 CLB to a revision 3.0 CBB without power
20. Connect the generator output to the lane 0 Rx SMP connectors on the CBB using the same cables used in calibration (if any adaptors are also used they must be minimal loss).
21. Connect the lane 0 Tx SMP connectors on the CLB to to a high speed oscilloscope via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
22. Set the generator output to an all zero pattern and turn the generator output on. Adjust the 2.1 Ghz differential noise component of the test equipment output to approximately 20 mV. Measure the DM average peak to peak amplitude over 1.6 X 10^6 unit intervals (at 8 GT/s) and adjust it to the range of 14-16 mv. Note that DM will be adjusted again in the final adjustments to achieve the target eye height and width.
23. Note the differential noise setting on the test equipment so that it can be recalled later.
24. Connect the end of the phase matched, low loss SMA cables (connected to the test equipment soruce and differential mode noise solution) directly to a real time oscilloscope.
25. Adjust the TX equalization of the test equipment so the measured TX equalization on the oscilloscope is P7. Measured preshoot must be 3.5 +/- .2 dB and measured de-emphasis must be 6.0 +/- .2 dB.
26. Connect the test equipment transmitter output to the lane 0 Rx SMP connectors on the CBB via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
27. Connect the lane 0 Tx SMP connectors on the CLB to to a high speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
28. Set all jitter and noise sources to the calibration values found above and have the test equipment transmit TX compliance pattern.
29. Capture 1.6 million unit intervals of data with the real time oscilloscope. Save the captured waveform to a file.
30. Analyze the waveform just captured using SigTest with the RX CTLE setting fixed to setting seven with the template for add-in card RX calibration including embedding the remaining portion of the channel (this is the same embedding as the system board TX test). Note the eye height and eye width.
31. Adjust the test equipment source Rj and/or DM until the measured eye height is 46 mV +0/-5 mV and the measured eye width is 41.25 +0/-2 ps over an average of three measurements, .
32. Note: it is preferable to get as close to the nominal values of 46 mV and 41.25 ps as possible.
33. Adjust the test equipment TX Equalization to the value manually requested by the vendor providing the device under test. The TX Equalization is calibrated to this value with the cables that will be connected to the CBB connected directly to the real time oscilloscope..
34. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the CBB main board are not connected to any receive lane SMP connectors on the CBB riser.

35. Insert the add-in card under test into a CBB without power. The signal source should be connected to the Rx lane under test on the CBB riser card, the error detector should be connected to the Tx lane under test on the CBB main board. Other TX lanes can be terminated with 50 ohm terminations or unterminated – as requested by the device under test provider.
36. Connect the 100 mhz reference clock output from the test equipment to the clock input SMP connectors on the CBB.
37. Power on the CBB.
38. Get the add-in card into loopback at 8.0 GT/s (see section 3.5 below).
39. Send the modified compliance pattern for the current data rate to the device under test.
40. Verify that the error detector found no more than one error in 10^{12} bits transmitted.
41. Power down the CBB and remove the add-in card.
42. Repeat the test with the test equipment TX EQ calibrated to P7. Verify that the error detector measures a bit error rate of E-4 or better in this case.
43. Repeat the test with thes test equipment TX EQ calibrated to to P8. Verify that the error detector measures a bit error rate of E-4 or better in this case.

    Note: Steps 43-46 are an informative short channel version of the test.
44. Repeat the test through step 33 using the same TX calibrated settings using the 2.0 CBB.
45. Repeat the test with the test equipment TX EQ calibrated to P1. Verify that the error detector measures a bit error rate of E-4 or better in this case.
46. Repeat the test with the test equipment TX EQ calibrated to P7. Verify that the error detector measures a bit error rate of E-4 or better in this case.
47. Repeat the test with thes test equipment TX EQ calibrated to P8. Verify that the error detector measures a bit error rate of E-4 or better in this case.

2.9. System Receive Jitter Tolerance Test

This test is run on all Card Electromechanical (CEM) form factor system boards. The test verifies that the system can function normally with an add-in card with jitter near the specification allowed limits and does not exceed the allowed receiver error rate in loopback mode.

Note: The test equipment error detector shall ignore SKP ordered sets when counting errors.

2.9.1. Starting Configuration

A programmable signal source such as a Bit Error Rate Tester (BERT), Arbitrary Waveform Generator (AWG) or other specialized test equipment is connected to the device under test (DUT) via a compliance base board. Since it is necessary to get the system board into loopback mode in order to perform this test, the signal source must be able to perform the sequence of steps outlined in Appendix A: Getting into Loopback for all data rates supported by the device under test.

2.9.2. Overview of Calibration Steps

The calibration is performed using the following steps. The test equipment provides the reference clocking during calibration (the system reference clock is not used):

1. Perform steps 1-25 of the Add-in Card Receive Jitter Tolerance Test.
2. Connect the test equipment transmitter output to the lane 0 Rx SMP connectors on the CLB via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
3. Connect the lane 0 Tx SMP connectors on the CBB to to a high speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
4. Set all jitter and noise sources to the calibration values found above and have the test equipment transmit TX compliance pattern.
5. Capture 1.6 million unit intervals of data with the real time oscilloscope. Save the captured waveform to a file.
6. Analyze the waveform just captured using SigTest with the RX CTLE setting fixed to setting seven with the template for system board RX calibration including embedding the remaining portion of the channel (this is the same embedding as the Add-in card TX test). Note the eye height and eye width.
7. Adjust the test equipment source Rj and/or DM until the measured eye height is 50 mV +0/-5 mV and the measured eye width is 45 +0/-2 ps over an average of three measurements.

   Note – These limits are less constrained than the limits in the PCI Express Card Electromechanical (CEM) specification to account for the clean reference clocks utilized by typical test equipment during calibration.
   It is preferable to get as close to the nominal values of 50 mV and 45 ps as possible.
8. Adjust the test equipment TX Equalization to the value manually requested by the vendor providing the device under test. The TX Equalization is calibrated to this value with the cables that will be connected to the CLB connected directly to the real time oscilloscope.
9. Make sure that the compliance toggle outputs are not connected to any receive lane SMP connectors on the CLB.
10. Insert the CLB into the system under test with the power off. The signal source shall be connected to the Rx lane under test on the back of the CLB, the error detector shall be connected to the Tx lane under test on the front of the CLB. The CLB 100 Mhz clock output from the system under test shall be connected to the test equipment and drive the test equipment transmissions after being filtered by a PCI Express 3.0 base specification compliant PLL or equivalent. Other TX lanes can be terminated with 50 ohm terminations or unterminated – as requested by the device under test provider.
11. Power on the system under test.
12. Get the system board into loopback at 8.0 GT/s (see section 3.4 below).
13. Send the modified compliance pattern for the current data rate to the device under test.
14. Verify that the error detector found no more than one error in 10^{12} bits transmitted.
15. Power down the system under test and remove the CLB.

2.10. Add-in Card Receiver Link Equalization Test for 8.0 GT/s

This test is run on all card electromechanical form factor add-in cards that operate at 8.0GT/s. The test verifies that the add-in card will correctly negotiate with its link partner to adjust the partner's transmitter equalization appropriately.

Note: The test equipment error detector shall ignore SKP ordered sets when counting errors.

The test equipment must respond to phase 2 requests to change TX Equalization within 500 nanoseconds as required by the PCI Express 3.0 base specification.

2.10.1. Starting Configuration

A protocol aware signal source and receiver such as a Protocol Test Card (PTC), Bit Error Rate Tester (BERT) or other specialized test equipment is connected to the device under test via a CBB. Since it is necessary to get the DUT into loopback mode through the link recovery state in order to perform this test, the protocol aware test equipment must be able to perform the sequence of steps outlined in Appendix A: Getting into Loopback for 8GT/s.

2.10.2. Overview of Test Steps

The test is performed by following these steps:

1. Perform steps 1-31 of the Add-in Card Receive Jitter Tolerance Test.
2. Insert the add-in card under test into the calibration CBB without power. The signal source should be connected to the Rx lane under test on the CBB riser card, the receiver of the protocol aware test equipment should be connected to the Tx lane under test on the CBB main board. Other TX lanes can be terminated with 50 ohm terminations or unterminated – as requested by the device under test operator.
3. Configure the protocol aware test equipment transmitter to initially transmit with preset P7 at 8.0 GT/s.
4. Power on the CBB.
5. Have the protocol aware test equipment train the DUT and negotiate to 8.0 GT/s.
6. Have the protocol aware test equipment run the link equalization protocol.
7. Have the protocol aware test equipment put the DUT into loopback.
8. Send the modified compliance pattern to the device under test
9. Verify that the error detector found no more than one errors in 1012bits transmitted.
10. Repeat the test with the protocol aware test equipment configured to initially transmit with preset P8 at 8 GT/s.
11. Repeat the test with the 2.0 CBB with the protocol aware test equipment configured to initially transmit with preset P8 at GT/s.
12. Repeat the test with the 2.0 CBB with the protocol aware test equipment configured to initially transmit with preset P7 at GT/s.

13. Repeat the test with the 2.0 CBB with the protocol aware test equipment configured to initially transmit with preset P1 at GT/s.

2.11. System Receiver Link Equalization Test for 8.0 GT/s

This test is run on all Card Electromechanical (CEM) form factor system boards that operate at 8.0GT/s. The test verifies that the system will correctly negotiate with its link partner to adjust the partner's transmitter equalization appropriately.

Note: The test equipment error detector shall ignore SKP ordered sets when counting errors.

The test equipment must respond to phase 3 requests to change TX Equalization within 500 nanoseconds as required by the PCI Express 3.0 base specification.

2.11.1. Starting Configuration

A protocol aware signal source and receiver such as a Protocol Test Card (PTC), Bit Error Rate Tester (BERT) or other specialized test equipment is connected to the device under test via a CLB. Since it is necessary to get the DUT into loopback mode in order to perform this test, the protocol aware test equipment must be able to perform the sequence of steps outlined in Appendix A: Getting into Loopback for 8GT/s.

2.11.2. Overview of Test Steps

The calibration is performed by following these steps:

1. Repeat steps 1-7 of the System Receive Jitter Tolerance Test.
2. Insert the calibration CLB into the system under test without power. The signal source should be connected to the Rx lane under test on the CLB, the receiver of the protocol aware test equipment should be connected to the Tx lane under test on the CLB. The CLB 100 Mhz clock output from the system under test shall be connected to the test equipment and drive the test equipment transmissions after being filtered by a PCI Express 3.0 base specification compliant PLL or equivalent. Other TX lanes can be terminated with 50 ohm terminations or unterminated – as requested by the device under test operator.
3. Configure the protocol aware test equipment transmitter equalization to match the initial TX EQ preset at 8 GT/s requested by the system board under test. This can be observed using separate protocol analysis equipment if necessary.
4. Power on the system under test.
5. Have the protocol aware test equipment train the DUT and negotiate to 8.0 GT/s.
6. Have the protocol aware test equipment run the link equalization protocol.
7. Have the protocol aware test equipment put the DUT into loopback.
8. Send the modified compliance pattern to the device under test.
9. Verify that the error detector found no more than one error in 1012 bits transmitted.

2.12. Add-in Card PLL Bandwidth

This test is run on all card electromechanical form factor add-in cards. The test verifies that the add-in card PLL bandwidth and peaking are within the limits allowed by the PCI Express specifications.

2.12.1. Starting Configuration

1. Connect one of the following two options to provide a reference clock with modulation for the PLL bandwidth test:
   a. Connect a signal generator to the noise injection port on the CBB. Note that the CBB may need to be modified to enable the port.
      The signal generator must be able to provide a signal that induces phase jitter on the reference clock from 0 to 25 MHz.

      Note: This approach will work with PLL designs that use only the rising edge of the reference clock.

   b. Connect an external source to the CBB reference clock input.
      The external source must be able to provide a 100 MHz reference clock signal with phase jitter from 0 to 25 MHz.

      Note: This approach will work with PLL designs that use both edges of the reference clock or only the rising edge of the reference clock.

2. Connect the output of transmit lane zero on the CBB main board to an instrument capable of measuring the transmitter frequency response as a function of the frequency of phase jitter on the reference clock.

2.12.2. Overview of Test Steps

The test is performed by following these steps:

1. Insert the add-in card under test into the CBB with the power off.
2. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the CBB main board are connected to receive lane zero (SMP connectors J18 and J2) on the CBB riser card via appropriate SMP to SMP cables.
3. Power on the CBB.
4. Measure the transmitter output and confirm that the transmitter output is the compliance pattern.
5. Apply modulation on the reference clock producing phase jitter from 0 to 25 MHz. The modulated reference clock is calibrated such that the measured reference clock phase jitter is within 20% of the limit allowed for a reference clock by the PCI Express 3.0 Specification. Measure the transmitter output on lane zero across this range.

6. Analyze the transmitter output and estimate the reference clock phase jitter frequency where the transmitter response is -3 dB. Also note the maximum amplitude of the transmitter output.
7. The -3 dB point must fall between the frequencies specified for the current data rate and the maximum peaking must be less than maximum allowed peaking for the current data rate
8. Repeat steps 4-7 with the amplitude set to ½ of the initial calibrated noise amplitude value.
9. Push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the add-in card under test) to move to the next data rate supported by the add-in card.
10. Repeat steps 4-9 until all data rates supported by the add-in card have been tested. For testing at 8 GT/s use the TX Equalization preset requested by the device under test.

2.13. Add-in Card PCB Impedance (Informative)

This test is run on all card electromechanical form factor add-in cards. The test verifies that the add-in card TX and RX path PCB differential trace impedance is in the range required by the PCI Express 3.0 Card Electromechanical Specification.

The differential impedance of the Tx and Rx lanes is checked with a TDR or equivalent to verify that the measured impedance of the PCB trace only (package is excluded) is within the CEM specification.

2.14. System Board PCB Impedance (Informative)

This test is run on all card electromechanical form factor system boards. The test verifies that the system board TX and RX path PCB differential trace impedance is in the range required by the PCI Express 3.0 Card Electromechanical Specification.

The differential impedance of some or all of the Tx and Rx lanes is checked with a TDR or equivalent to verify that the measured impedance of the PCB trace only is within specification.

A

Appendix A. Getting into Loopback

In order to perform receiver tolerance tests the product under test must first be trained and directed to enter the Loopback state. This is done by taking the product through the state machine from Detect via Polling and Configuration to the Loopback state using the protocol as specified in PCI Express Base Specification, Rev 2.0.

A.1. Loopback Training

The state transitions needed to get the device under test into loopback mode are pictured in Figure 1:

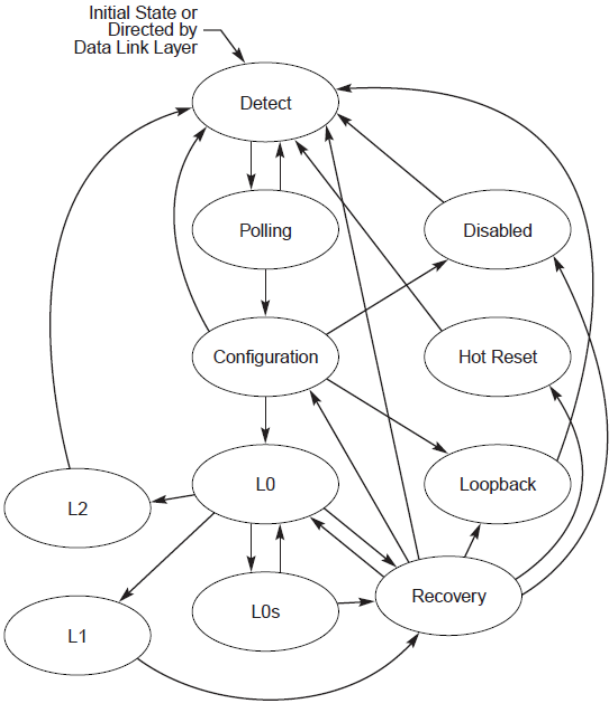

Figure 1: Main State Diagram for Link Training and Status State Machine

A.1.1. Step by Step Sequence

The following sequence of steps will cause the device under test to enter loopback state:

1. Start sending TS1 with PAD (K23.7) which takes the product into the Polling.Active state.

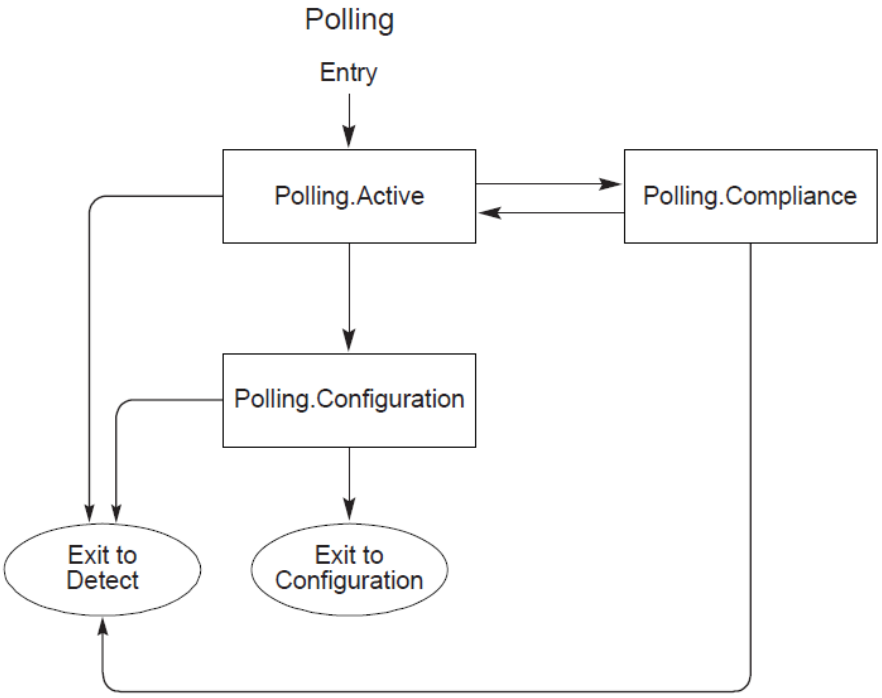

Figure 2: Polling Substate Machine

2. Polling.Configuration is reached after >1024 TS1 have been transmitted and 8 consecutive TS1 or TS2 with Pad or Loopback bit asserted have been received.
3. The Configuration state is entered after 8 consecutive TS2 with Pad have been received and 16 TS2 have been transmitted after 1 TS2 has been received.
4. Speed negotiation is initiated by sending TS1 at 2.5 GT/s advertising the supported speeds.
5. Electrical idle for more than 1 ms allows the product to adjust to the requested speed unless the requested speed is 2.5 GT/s.
6. Two consecutive TS1 at the requested speed with Loopback bit asserted takes the product to the Loopback state.

A.1.2. Loopback Training at 2.5 GT/s

The sequence necessary to cause a device under test to enter loopback at a data rate of 2.5 GT/s is shown in Figure 3:

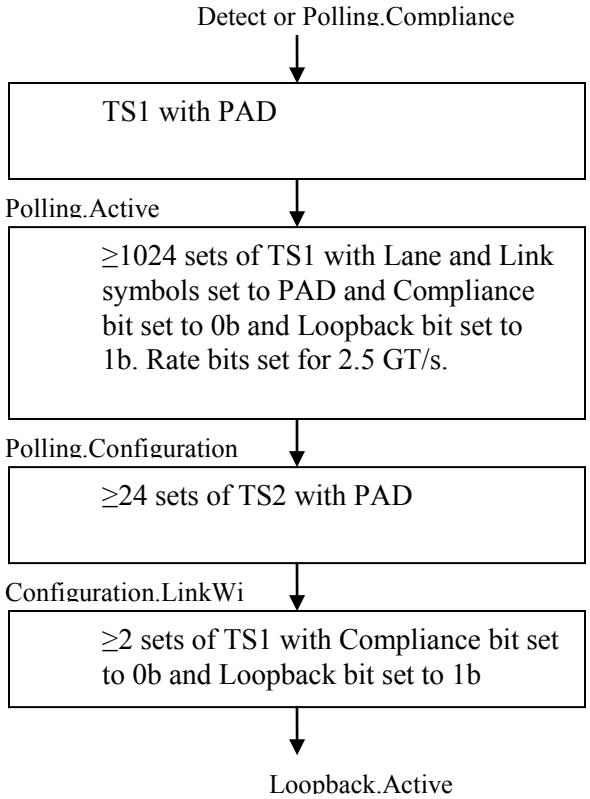

Figure 3: 2.5 BT/s Loopback Training Sequence

A.1.3. Loopback training at 5.0 GT/s

The sequence necessary to cause a device under test to enter loopback at a data rate of 5.0 GT/s is shown in Figure 4:

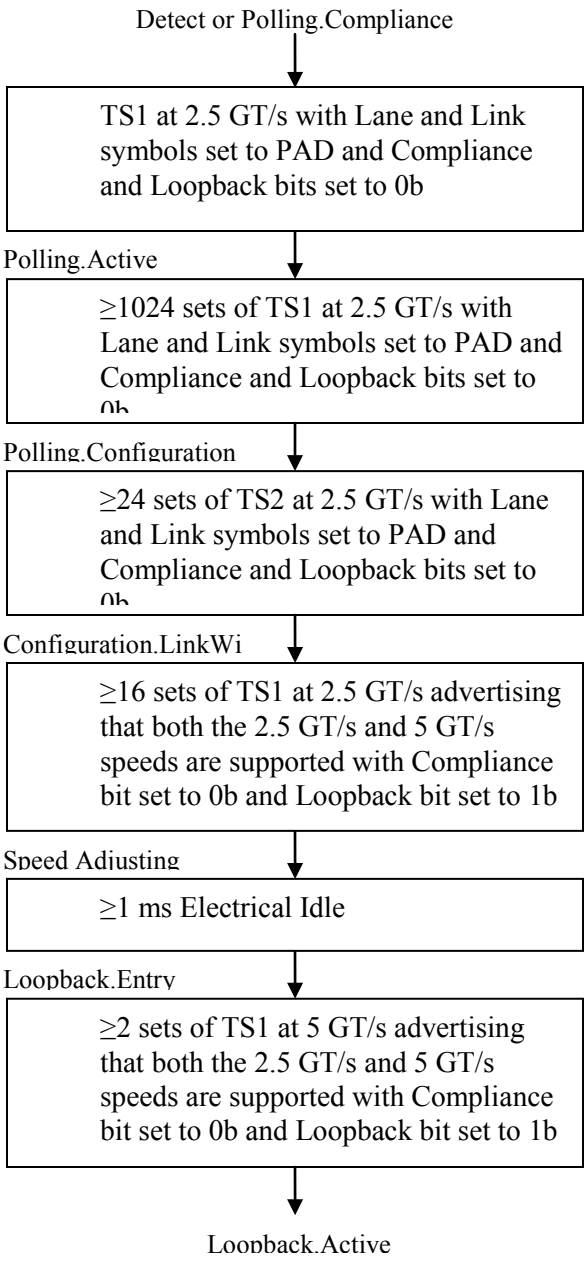

Figure 4: 5.0 GT/ s Loopback Training Sequence

A.1.4. Loopback training at 8.0 GT/s

The sequences that will be used to cause a device under test to enter loopback through the configuration link state and through the recovery link state at a data rate of 8.0 GT/s are specified in the PCI Express 3.0 Link Test Specification.

B

Appendix B. Transmitter Signaling Analysis

The process of analyzing transmitter output to determine the signal quality and, ultimately, the ability of a particular transmitter to operate with any receiver that complies with the receiver specification is an intricate process. While the Dual Dirac method used in this analysis is well documented elsewhere, it is useful to describe this analysis technique as used for transmitter testing here.

B.1. Outline of Tx signal analysis

Within the context of PCI Express, transmitter electrical compliance is computed by analyzing a waveform captured using a high-speed, real time oscilloscope. Because of the high frequency nature of the signal being analyzed, the oscilloscope must have a bandwidth of at least 6 Ghz and a sample rate of at least 20 GS/s (50 ps sample interval) for 2.5GT/s signaling and a bandwidth of at least 12 Ghz and a smple rate of at least 40 GS/s (25 ps sample interval) for 5.0GT/s and 8.0GT/s signaling.

The captured waveform is optionally conditioned by a specified test channel and specified receiver equalization (CTLE and DFE). The resulting waveform is then analyzed for timing jitter and minimum and maximum signal amplitude.

Timing analysis is based on a specified target Unit Interval (UI) and, when doing random jitter (Rj) and deterministic jitter (Dj) separation, timing uncertenty extrapolated to a Bit Error Rate (BER) than can be significantly greater than the BER computed directly from the measured data.

Signal amplitude analysis is based on the measured waveform amplitude as modified by any specified waveform conditioning (test channel embedding and Rx equalization) and related to timing defined by the specified target UI.

B.1.1. Input Waveform Conditioning

Three different forms of waveform conditioning can be applied to the input waveform:

B.1.1.1 Channel Embedding

The channel is defined by S-Parameters. The channel description is read in and stored internally. When a waveform is presented for processing, the waveform is converted to the frequency domain then multiplied with the channel description, The result of the multiplication is converted back to the time domain.

The waveform is input as two single-ended acquisitions or a single differential acquisition and output as a single, differential waveform.

B.1.1.2 CTLE Equalization

Continuous Time Linear Equalization (CTLE) is performed in a similiar manner. The input waveform is transformed into the frequency domain. The CTLE parameters (AC/DC gain, one zero frequency and two pole frequencies) are used to define an equivalent frequency domain response and the input waveform is convolved with the CTLE response. The result of the convolution is converted back to the time domain.

Multiple CTLE parameter sets can be specified. The waveform resulting from each CTLE filter then has DFE applied. The optimal CTLE (and, if specified, DFE) parameter set is determined by examining the resulting transition and non-transition eye heights and widths for each set of CTLE parameters. Once the optimal CTLE (and DFE, if specified) parameter set has been determined, it is applied to the entire waveform.

B.1.1.3 DFE Equalization

Decision Feedback Equalization (DFE) is performed strictly in the time domain. The eye area is used to find the optimal DFE tap value between – 30 and + 30 mV (inclusive).. Once the taps are known, each sample point of the input waveform is modified according to the tap values and the state (logic 0 or logic 1) of the waveform at each tap location.

B.1.2. Crossover and Interval Determination

Once the input waveform conditioning has been performed, the input waveform is analyzed to determine the time at which the signal crosses the zero Volts threshold. The crossover time is determined using linear interpolation between the two sample points closest to the zero crossing.

The interval between successive crossovers is computed by subtracting the crossover time at the beginning of the interval from the crossover time at the end of the interval: $Interval_n = Crossover_{n+1} – Crossover_n$. Information allowing a given interval to be traced back to its location within the input waveform is retained.

In most cases, (all cases except when the input waveform is a toggle pattern) the input waveform will contain multi-bit intervals. To meet the analysis requirements, the multi-bit intervals need to be replaced with multiple single bit intervals. The period of each added interval is merely the period of the original, multi-bit interval divided by the number of unit intervals represented.

Since this step is where the bit length of each interval is determined, any pattern checks that have been specified are performed at this time.

B.1.3. Time Interval Error (or Phase Jitter) Determination

The jitter per edge and the subsequent Time Interval Error (TIE) are computed based on the clock period for each unit interval in the input data. For single port measurements (as used in Add-In Card analysis) a single clock value is computed for the entire data record. For dual port analysis (as used in System Board analysis) the clock for each unit interval in the data reacord is computed from the supplied clock waveform. These methods are described below.

B.1.3.1 Single Port (Add-In Card) Jitter Determination

No explicit clock information is provided for single port analysis so the clock must be determined from the data waveform. Two methods are available for doing this, least squares fit and mean interval.

B.1.3.2 Least Suqares Fit Clock Interval Method

The least squares fit method plots the interval duration on the Y axis against the interval on the X axis. The least squares fit line is computed and the slope of this line is used as the unit interval period for jitter determination.

B.1.3.3 Mean Clock Interval Method

The mean interval method merely finds the mean of all the intervals and uses this value as the unit interval period for jitter determination.

B.1.3.4 Single Port Data Waveform Phase Jitter Computation

The jitter at each interval is found by subtracting the unit interval period (as computed above) from each interval. It is important to note that the resulting jitter value can be either positive (interval is greater than unit interval) or negative (interval is less than unit interval).

Finally, this jitter data is converted into phase jitter or the Time Interval Error (TIE) by accumulation; that is, the jitter at each unit interval is summed to give the TIE at that UI: $TIE_0 = J_0$, $TIE_n = TIE_{n-1} + J_n$.

B.1.3.5 Dual Port (System Board) Jitter Determination

For dual port analysis, the system clock is captured simultaneously with the data. Both the clock waveform and the data waveform are input to the analysis software and the data waveform is processed as described above in sections 4.1.1 through 4.1.2.

The clock waveform is processed in a similar maner, but without any waveform conditioning. Further, in general, the crossover times of only the rising edge of the clock waveform are interpolated. The resulting crossover periods (from rising edge to rising edge of the clock signal) are then interpolated to the correct number of unit intervals.

At this point, there is an array of unit interval values for the data and an array of unit interval value for the clock.

B.1.3.6 Phase-Locked Loop (PLL) Filter of Clock Jitter

Several different PLL filter values are specified to constrain the effect of the transmit and receive PLLs on the clock. For each specified filter value, the clock values are filtered according to each set of PLL filter parameters. The jitter values are computed for each filter specified and the total jitter (Tj) is used to determine which results to retain. The largest Tj found is retained as the result for all clock filter values.

B.1.3.7 Clock to Data Skew

Even though the clock waveform is captured simultaneously with the data waveform, there may be delay between the clock and data waveforms due to different routing on the system board. The CEM spec defines a maximum for this skew. To compensate for this possible skew, the analysis is done at three different values of clock to data skew:

1. Clock delayed by maximum allowed amount with respect to the data.
2. No delay introduced between clock and data.
3. Data delayed by maximum allowed amount with respect to the clock.

Obviously, any delay must be an integer number of unit intervals so the number of unit intervals closest the the specified maximum skew is used to offset the clock and data values.

As with the PLL filter values, the total jitter is computed for all three delay combinations and the worst case Tj is retained as the final result. If there are three filters specified there will be three skew cases for each filter thus the algorithm to find the total jitter will be executed nine times in all.

B.1.3.8 Dual Port Data Waveform Phase Jitter Computation

The jitter at each interval is found by subtracting the clock interval from the data interval. The clock interval has been filtered (as noted in section 4.1.3.6 above) and clock to data skew has been applied (as noted in section 4.1.3.7 above). The phase jitter or Time Interval Error (TIE) is computed as described for the single port data waveform jitter in section 4.1.3.4 above.

B.1.4. Jitter Determination

The phase jitter, whether computed using the single port or dual port method, is used to compute the total jitter and, by application of the Dual Dirac method, the deterministic jitter.

B.1.4.1 Phase Jitter High Pass Filter

A high pass filter is applied to the phase jitter based on parameters specified. The filter can be a brick wall filter or a simple first or second order filter. The cut-off frequency, damping factor (for second order filters) and brickwall floor value (for brick wall filters) are specified for this filter.

B.1.4.2 Jitter Metrics

At this point, the total jitter for each unit interval represented in the input waveform is known. Jitter metrics such as maximum peak-to-peak jitter are computed and saved for display later.

B.1.4.3 Dual Dirac Fitting

With the suitably filtered jitter values available, first the Probability Distribution Function (PDF) then the left and right Cumulative Distribution Functions are computed. The PDF is found by forming a histogram of the jitter values around zero; the number of bins to be used in the histogram is supplied as a parameter to this function. The range of jitter values determines the size of each bin in picoseconds.

The cumulative distribution functions are found by accumulating the PDF from one end to the other. The left side CDF is generated by by accumulating the PDF from left to right (index 0 through index *n*), the right side CDF is gnereated by accumulating the PDF from the right to the left (index *n* through 0).

The left and right CDF values are converted to Q space using the complementary inverse error function. Specifically, the CDF is multiplied by two, converted by the complementary inverse error function then multiplied by the square root of two. The complementary inverse error function has the interesting property of mapping a Gaussian distribution into a straight line. Thus a Gaussian can be extrapolated in Q space merely by extending a straight line. This is done for both left and right cumulative distribution functions using a slope (Rj) computed from the frequency domain phase jitter.

C

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